REMARKS

This paper responds to the Office Action mailed on June 15, 2005.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-12 and 23-64 are now pending in this application.

§102 Rejection of the Claims

Claims 1-3, 5, 6, 8-11, 13-22, 25, 27-29, 31, 33-35, 38, 39, 41, 44, 46, 47, 50, 52, 53, 56, 58, 59, 62, and 64 were rejected under 35 U.S.C. § 102(e) for anticipation by Pan (U.S. Patent No. 5,739,066). Applicant respectfully traverses this rejection.

The cited Pan reference discloses a method of preventing the reduced gate line conductivity that results from the gate dielectric damage repair oxidation step (col. 1, lines 27-42). The sidewalls of the gate 16 are protected by blanket deposition of nitride 32 (col. 3, line 25 and Fig. 2) which is anisotropic etched to form the sidewalls 34 and 36 (col. 3, line 33). The sidewall spacers 34 and 36 protect the sides of the gate 16 from the re-oxidation repair of gate oxide 14 (col. 3, line 44 and Fig. 8).

Applicant respectfully submits that the cited reference does not disclose each and every feature of the claimed invention, and thus can not anticipate the present claims.

In particular, the cited reference does not disclose at least the claimed feature of "*...selectively depositing a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls...*", as recited in claims 1 and 6, which thus are patentably distinct over Pan. Pan does not *selectively deposit* anything, and uses the *blanket* deposition of the nitride 32, as discussed at col. 3, line 25, and shown in figure 2. Similar teachings are found at least at layer 38 in figures 4 and 6, and the associated text at col. 4, lines 10-20, and lines 33-41.

The cited reference does not disclose at least the claimed feature of "*... selectively forming a first oxidation barrier comprising silicon nitride or an amorphous silicon film only on the sidewalls of the gate...*", as recited in claim 9. The reasoning is similar to that given above with reference to claims 1 and 6, namely that Pan does not selectively deposit anything.

The cited reference does not disclose at least the claimed feature of "*...avoiding depositing the thin silicon nitride on the insulating layer disposed above the source and the drain*

region...", as recited in claim 11. Pan does a blanket deposition of nitride 32, and thus fails to avoid depositing the nitride on the insulating layer above the source and drain.

The cited reference does not disclose at least the claimed feature of "*...forming a spacer comprising silicon nitride or an amorphous silicon film covering the surface of the feature and terminating at a location adjacent to the boundary wherein the spacer is not in contact with the oxide layer...*", as recited in claim 41. The disclosed spacer 36 of Pan is clearly in contact with the oxide layer 14, as shown in figure 3.

The cited reference does not disclose at least the claimed feature of "*...forming a spacer comprising silicon nitride or an amorphous silicon film only on a substantially vertical portion of the surface ...*", as recited in claim 47. Pan forms the layers 32 and 38 on all the surfaces of the gate 16, and not only on the vertical portion. The Pan structure has a final arrangement having nitride 30 on the top horizontal surface of the gate 16, and thus Pan can not anticipate the present claims.

The cited reference does not disclose at least the claimed feature of "*...oxide forming a gap at a boundary between the feature and the first layer of oxide ...*", as recited in claim 53. As discussed above, the cited reference does not have a gap at the interface of the vertical and horizontal dielectric layers, and thus can not anticipate the claim.

The cited reference does not disclose at least the claimed feature of "*...depositing a spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of the electrode, the spacer extending to and terminating adjacent to a boundary between the first layer of oxide and the sidewalls of the electrode...*", as recited in claim 59. Pan neither deposits the nitride only on the sidewalls, nor terminates the film above the gate oxide layer.

The dependent claims are held to be patentably distinct over the cited Pan reference at least as depending from base claims shown above to be distinct over Pan, and further as having additional patentable features over the base claims, not found in the cited reference. In view of the above discussion, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 4, 7, 12, 26, 30, 32, 36, 37, 40, 42, 45, 48, 51, 54, 57, 60, and 63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pan in view of Hurley (U.S. Patent No. 6,350,708). Applicant respectfully traverses this rejection.

The cited reference of Pan has features discussed above with reference to the anticipation rejection. The cited reference of Hurley discloses that the different incubation periods (col. 1, lines 27 and 41; col. 2, lines 7 and 33) for different surfaces at the beginning of a nitride deposition process may be resolved by a pre deposition of a monolayer of silicon on the surface of the wafer (col. 1, line 29; col. 2, lines 42 and 58). After the silicon pre-deposition the nitride layer grows at "a substantially equivalent rate independent of the surface type" (col. 2, lines 53-54). Nothing in Hurley describes or suggests the use of a selectively deposited layer. The cited reference of Hurley is used in the outstanding Office Action to show that incubation times are known in the art.

Applicant respectfully submits that Hurley teaches away from the claimed invention of selectively depositing the spacers on the sidewalls of the electrode by teaching how to initiate the deposition on "different wafer surfaces", such as all surfaces, as discussed at col. 2, lines 44-60.

Applicant further submits that the Examiner has not meet the burden of showing a reason why one of ordinary skill in the art should make the suggested combination of references of Pan and Hurley. This is true since Hurley suggests a method of creating uniform thickness layers, while Pan suggests a method to vertically (i.e., anisotropically) remove all the layer deposited on horizontal surfaces, and has no sensitivity to layer thickness uniformity.

Applicant further respectfully submits that the cited reference does nothing to cure the above noted deficiencies of Pan, specifically the failure to disclose the claimed feature of "*...selectively depositing a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls...*", as recited in claims 1 and 6, with similar recitations in the other independent claims, from which the claims in question depend, either directly or indirectly. Applicant submits that even if there were proper motivation to make the suggested combination, the result would still not suggest at least the above noted claimed feature. In view of the above discussion, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 23, 32, 37, 42, 48, 54, and 60 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pan in view of Hurley and further in view of Woo et al. (U.S. Patent No. 4,774,201). Applicant respectfully traverses this rejection.

The cited references of Pan and Hurley have features discussed above with reference to the previous rejections. The cited reference of Woo is used in the outstanding Office Action to show that silicide reoxidation is known.

Applicant respectfully submits that the cited Woo reference does nothing to correct the deficiencies of the suggested combination of Park and Hurley as discussed above with reference to the previous rejection. Specifically, the suggested combination of references does not describe or suggest at least the claimed feature of "*...selectively depositing a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of each of the one or more features ...*", as recited in claim 1, from which claim 23 depends. As previously discussed the cited references, whether taken alone or in any combination, do not suggest selective deposition.

Similar arguments apply to the other independent claims as used in claim 1. The dependent claims are held to be in patentable condition at least as depending from base claims shown above to be patentable over the suggested combination of references. In view of the above discussion, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 24, 33, 38, 43, 49, 55, and 61 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pan in view of Liao et al. (U.S. Patent No. 5,480,830). Applicant respectfully traverses this rejection.

The cited reference of Pan has features discussed above with reference to the previous rejections. The cited Liao reference is used in the outstanding Office Action to show that it is known to have an electrode made of undoped silicon.

Applicant respectfully submits that the Liao reference does nothing to correct the deficiencies of the Park reference discussed above. Specifically, the suggested combination of reference neither describes nor suggests at least the claimed features of "*...selectively depositing*

a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of each of the one or more features ...", as recited in claim 1, from which claim 24 depends.

As previously discussed the cited references, whether taken alone or in any combination, do not suggest selective deposition.

Similar arguments apply to the other independent claims as used in claim 1. The dependent claims are held to be in patentable condition at least as depending from base claims shown above to be patentable over the suggested combination of references. In view of the above discussion, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 14 Oct '05

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of October, 2005.

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